



Bluetooth Low-energy Integrated Module for SME's (BLIM4SME)

Call: FP7-SME-2013, Research for the Benefit of SMEs

Grant Agreement Number: 605264

Project start date: 01/11/2013

Duration: 24 months

Project coordinator:
RTD Talos, Cyprus

Partners:

RivieraWaves SAS (RW), France

Prisma Electronics ABEE (PRISMA), Greece

Nordic Components OY (NORDIC), Finland

Teknologian Tutkimuskeskus VTT (VTT), Finland

CSEM Centre Suisse D'electronique Et De Microtechnique Sa - Recherche Et Developpement (CSEM),
Switzerland

Title of the document	Deliverable D2.1 RF, digital IC and RF IPD module preliminary datasheets
Dissemination level	PU – Public
Contractual date of delivery	31/07/2014
Work Package	WP2 - RF IC
Prepared by (Lead Partner)	CSEM
Partners involved	All
Authors	

Revision History

Version	Date	Changed page(s)	Cause of change	Partner
v1	31/07/2014	All	Creation of the document	CSEM

Disclaimer: The information in this document is subject to change without notice. Company or product names mentioned in this document may be trademarks or registered trademarks of their respective companies.

All rights reserved.

The document is proprietary of the BLIM4SME consortium members. No copying or distributing, in any form or by any means is allowed without the prior written agreement of the owner of the property rights.

This document reflects the authors' view. The European Community is not liable for any use that may be made of the information contained herein.

Contents

Executive Summary	4
Preamble	5
1 IPD module preliminary datasheet	6
2 RF IC preliminary datasheet	9
List of Tables.....	13
List of Figures.....	13

Executive Summary

This document consists in the deliverable D2.1. “RF, digital IC and RF IPD module preliminary datasheets”. Its principle is to present preliminary specification of IC and IPD module after important part of the design is performed, based on former D1.1 “BLIM4SME architecture, technical and Demonstrator Specs.” deliverable. The IC datasheet part will be updated and enriched with characterization results in D2.2 “RF and digital IC first samples characterization report” following future IC integration. The IPD module datasheet part will be updated and enriched with characterization results in D3.2 “First RF IPD module report”.

The D2.1 is structured as follows:

- An introduction section introduces the two following chapters with a recall of architecture.
- The IPD module datasheet section.
- The IC preliminary datasheet section.

Preamble

About the Project Results & terminology

For sake of readability of this document, and for respecting coherence with the DoW, the Project Results are summarized in this subsection (see also DoW table 3.2.2a). The correspondence with the technical/technology terminology used in this document is also provided (see also DoW section 1.1.2).

Result 1: BLE Generic Module:

This concerns in the BLE Generic Module in the form of a PCB that will embed the outcome(s) of Result 2 below, with additional features (e.g. sensors, etc).

The principal exploiter of this Result 1 is PRISMA.

Result 2: RF IPD Module:

This concerns the radio module that embeds IPD technology and which will be provided in two forms in the project:

- The **COTS module** which uses off-the-shelf radio components. Besides being a direct outcome of Result 2, it also serves for benchmark purposes for the **BLIM module** described below.
- The **BLIM module** which uses the BLIM4SME radio technology of Result 3 below.

The principal exploiter of this Result 2 is NORDIC.

Result 3: RF IC IP:

This concern the RF IC platform developed specifically in the project, and which is referred to as the **BLIM RF IC IP** or **BLIM chip**. This outcome is in the form of a silicon IP which will be integrated in the project as a chip.

The principal exploiter of this Result 3 is RW.

1 IPD module preliminary datasheet

The IPD modules are Bluetooth 4.1 Low Energy (marketed as Bluetooth Smart) BGA micro-modules with integrated Baseband Controller, Radio Transceiver and Antenna, c.f. Figure 1 below.

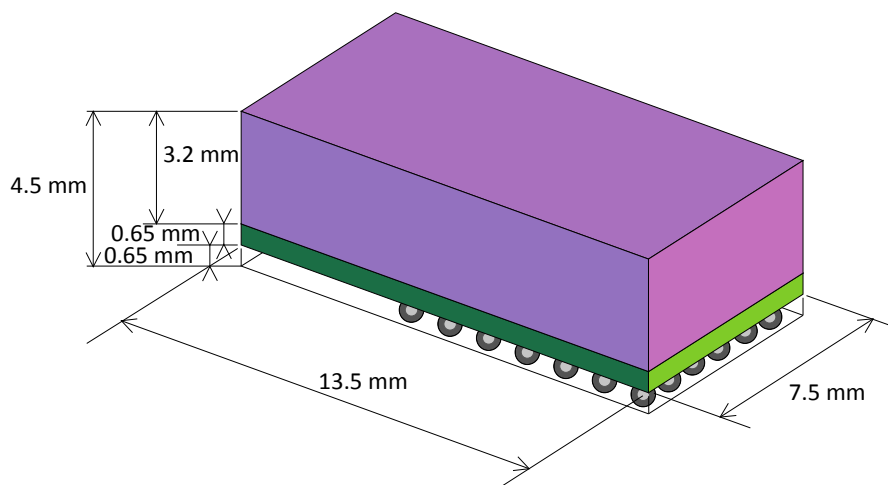


Figure 1: Modules dimensions

Parameter		
Communication standard	Bluetooth 4.1 Low Energy (2.45 GHz)	
Dimensions	13.5 x 7.5 x 4.5 mm (without additional surface for additional ground plane or exclusion volume)	
Interface	UART / SPI / I2C / ADC / PWM / GPIO	
Voltage supply	2.4-3.6 V	
Peak current	5 mA COTS module	3 mA BLIM module
Communication range	300 m free-space typical	

Table 1: IPD module specification summary

Upper protocol layers firmware, and possibly limited memory application software, is running on integrated ARM Cortex M0.

Two different modules are considered (c.f. D1.1):

- The **COTS module**, which uses off-the-shelf radio components. Besides being a direct outcome, it also serves for benchmark purposes for the BLIM module described below.
- The **BLIM module**, which uses the RF IC (BLIM IC) also developed in the project, described in following section of this document, and an off-the-shelf ARM Cortex M0 with 128 kB of Flash memory and very limited component count.

The goal is to build these modules upward compatible, at functionality, interface, as well as mechanically. Both are integrating same **antenna** and **IPD component** that implements filtering and antenna impedance matching.

The modules are planned to be mounted, amongst other possibilities, on **generic module** specified in D4.1 deliverable. This **generic module** supports additional sensors and targets, again amongst other possibilities, end-of-project demonstration.

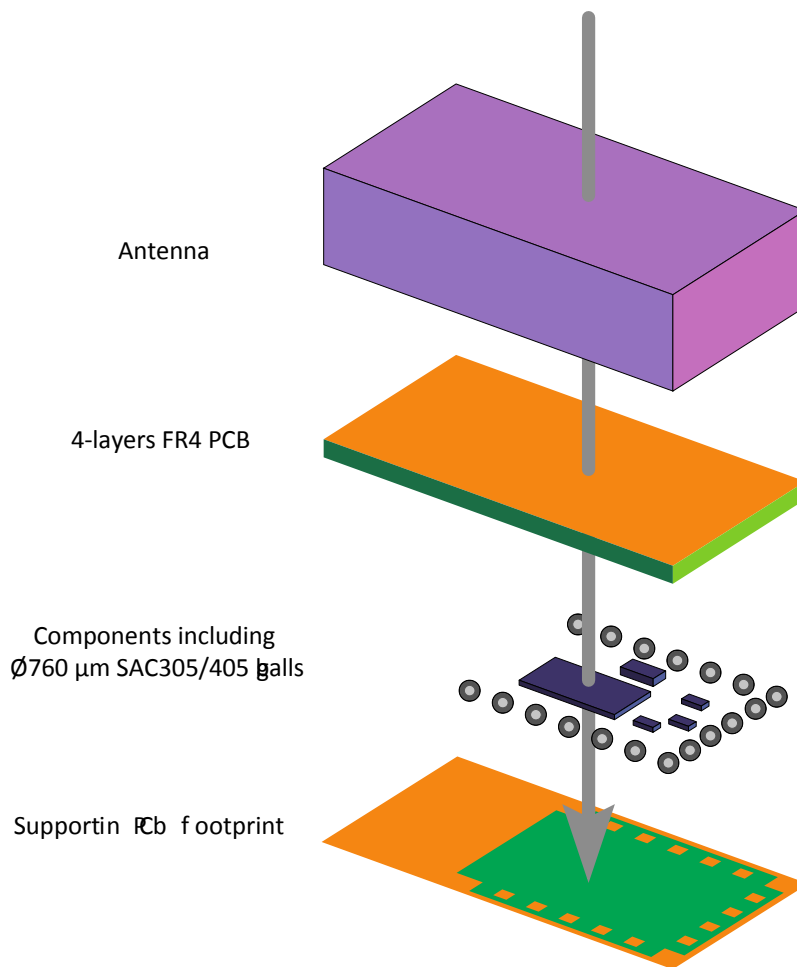


Figure 2: BLIM4SME exploded view

The antenna does not constrain the supporting PCB outside the underlying 13.5 x 7.5 mm footprint with a 7.5 x 4.5 mm ground plane and > 0.2 mm surrounding ground ring, c.f. Figure 3 below:

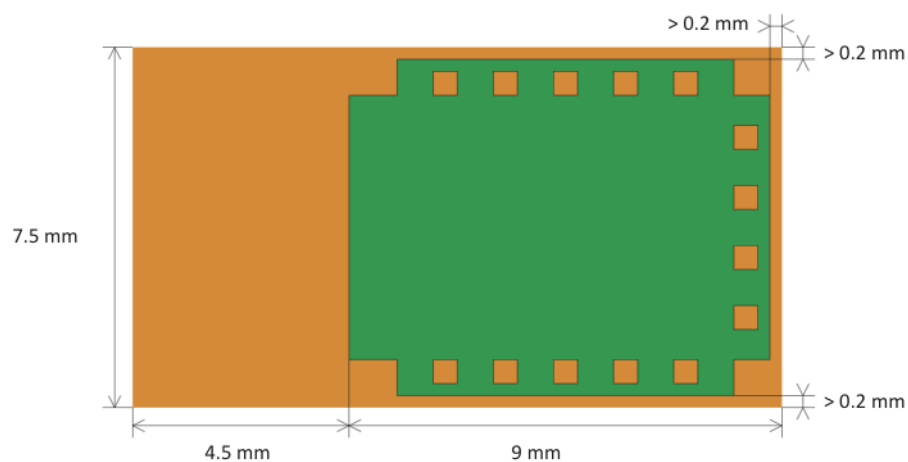


Figure 3: Modules PCB footprint

Common pinning of the 0.127 mm pitched BGA IPD module:

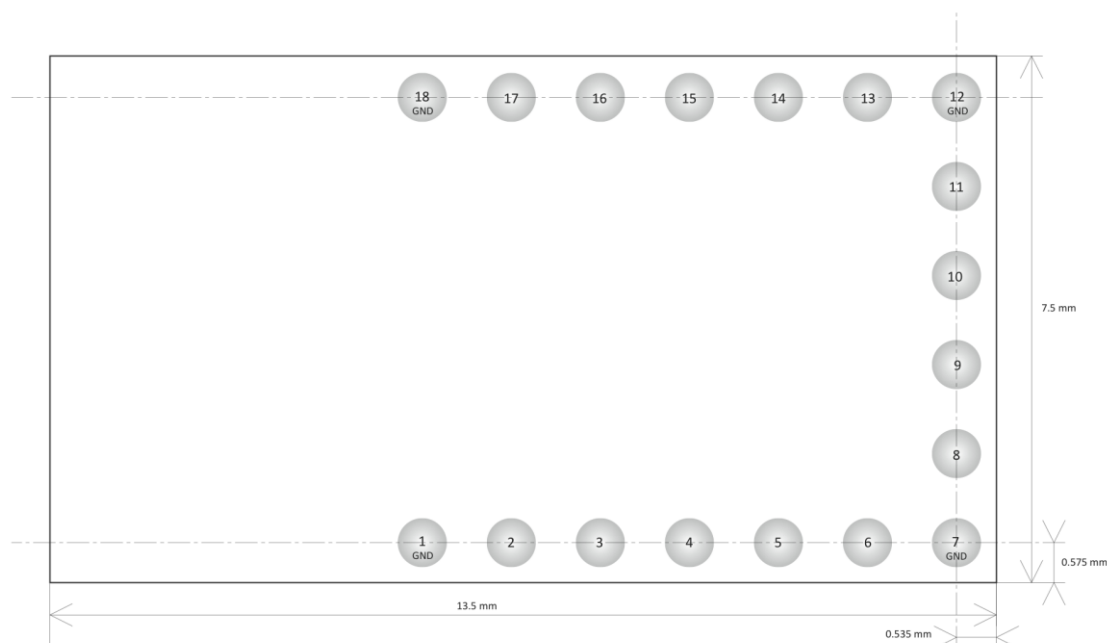


Figure 4: Modules pinning

Ref.	IO Type		Description
1	S	Module ground connection	Module ground connection
2	DIO	ADC_IN0 / UART1_TX / PWM0 / GPIO0	A priori main UART for communication with host controller (general purpose analog or digital IO if not used)
3	DIO	ADC_IN1 / UART1_RX / PWM1 / GPIO1	
4	DIO	ADC_IN2 / UART3_TX / PWM2 / GPIO2	General purpose analog or digital IO
5	DIO	I2C_SCL / UART2_TX / GPIO3	A priori I2C interface (general purpose digital IO or secondary UART possible if not used)
6	DIO	I2C_SDA / UART2_TX / GPIO4	
7	S	GND	Module ground connection
8	DIO	SPI_NSS / GPIO5	SPI interface, for BLIM module, used internally for communication between RF IC and microcontroller (general purpose digital IO if not used in slave)
9	DIO	SPI_SCK	
10	DIO	SPI_MISO	
11	DIO	SPI_MOSI	
12	S	Module ground connection	Module ground connection
13	DIO	SWCLK / GPIO6	Serial Wire Debug interface clock (JTAG - similar)
14	DIO	SWDIO / GPIO7	Serial Wire Debug interface data (JTAG - similar)
15	DIO	NRESET	RESET active low
16	DIO	ADC_IN3 / UART3_RX / PWM3 / GPIO8	General purpose analog or digital IO
17	S	VDD	2.4-3.6 V positive voltage supply
18	S	GND	Module ground connection

Table 2: Preliminary BLIM module IO list

2 RF IC preliminary datasheet

The BLIM RF IC integrates the hardware part of an RF transceiver compliant with Bluetooth 4.1. The software part is intended to be implemented into a companion microcontroller communicating with the BLIM RF IC via SPI and IRQ.

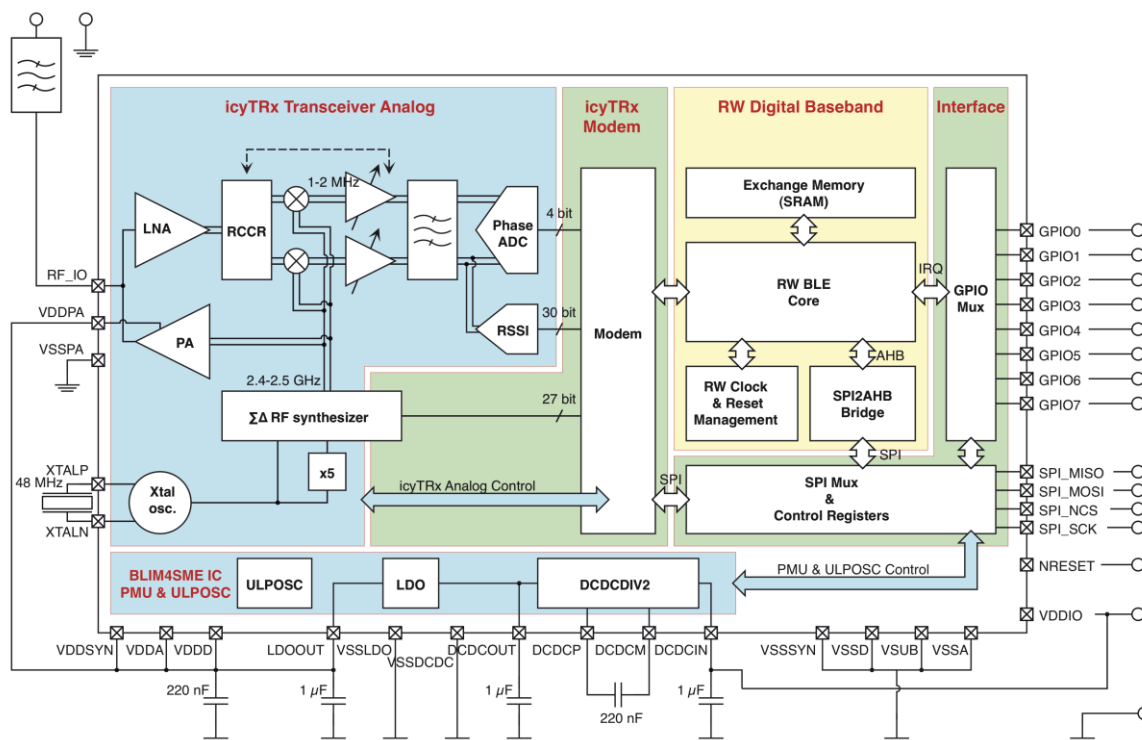


Figure 5: Top-level BLIM RF IC circuit block diagram

Parameter	
Communication standard	Bluetooth 4.1 Low Energy (2.45 GHz)
IC dimensions	1.65 x 1.45 x 0.38 mm
External components	One 48 MHz quartz Xtal, down to 1.2 x 1.0 x 0.3 mm ¹ , two 220 nF ceramic capacitors, down to 0.4 x 0.2 x 0.3 mm (01005), three 1 μF ceramic capacitor, down to 0.6 x 0.3 x 0.35 mm (0201).
Interface	RF: single 50 Ω interface, Digital: SPI & GPIO
Voltage supply	2.4-3.6 V
Transmission	0 dBm, 4.5 mA, 5 μs transient after 0.5 ms Xtal osc. startup
Reception	-97 dBm, 3.0 mA, 15 μs transient after 0.5 ms Xtal osc. startup
Standby current	300 nA Including RTC based on 32 kHz osc. and 4 kB RAM leakages

Table 3: IPD module specification summary

¹ E.g. <http://www.abracon.com/Resonators/ABM13.pdf>

The BLIM RF IC is the assembly in TSMC 65 nm of two pre-existing IP:

- The CSEM's **icyTRX-65** Bluetooth Low Energy RF transceiver implementing the **Physical Layer**, The **Bit Stream Processing** and **Air interface Packet assembly and disassembly** (i.e. Packet Data Unit insertion / extraction with Access Address recognition and CRC check). It also addresses 802.15.4 or proprietary standard from 62.5 kbps to 4 Mbps.
- The RivieraWaves's Bluetooth Low Energy 4.1 protocol engine implementing the **Bit Processing, Advertising / Data / Control Packets** type support, **Encryption, Frequency Hopping** management, **Time Division Multiple Access** events formatting and synchronization, **Broadcast / Central / Observer / Peripheral** classes support and **Real-Time-Clock** management. Simple and optimized hardware interface is implanted for the software-implemented protocol part. The BLE Software Stack, running in "full-embedded mode" where the lower, upper, profile and protocol stacks run on the same microcontroller, is divided into the following components:
 - LL: Link Layer
 - L2CAP: Logical Link Controller and Adaptation Protocol
 - SMP & ATT: Security Manager Protocol and Attribute Protocol
 - GATT / GAP: Generic Profiles
 - LE Profiles: BLE specific profiles (Findme, Proximity, Thermometer, Running, Cycling, HID, etc.)

The resultant IC also implements dedicated Power Management and Ultra-Low-Power time keeping functionalities:

- A capacitive DC-DC voltage converter supplies the IC core from the 2.4-3.6 V supply voltage for minimum peak current and component size and cost.
- An all integrated 32 kHz oscillator to eliminate a quartz Xtal for minimum size and cost.

The total assembly targets state-of the art performances with minimized power consumption in active and standby modes thanks to optimized architecture, clock gatings, power domains, etc.

Choice has been made to not co-integrate the companion controller in order to provide maximum flexibility and evolution of controller choice with minimum silicon footprint for cost minimization.

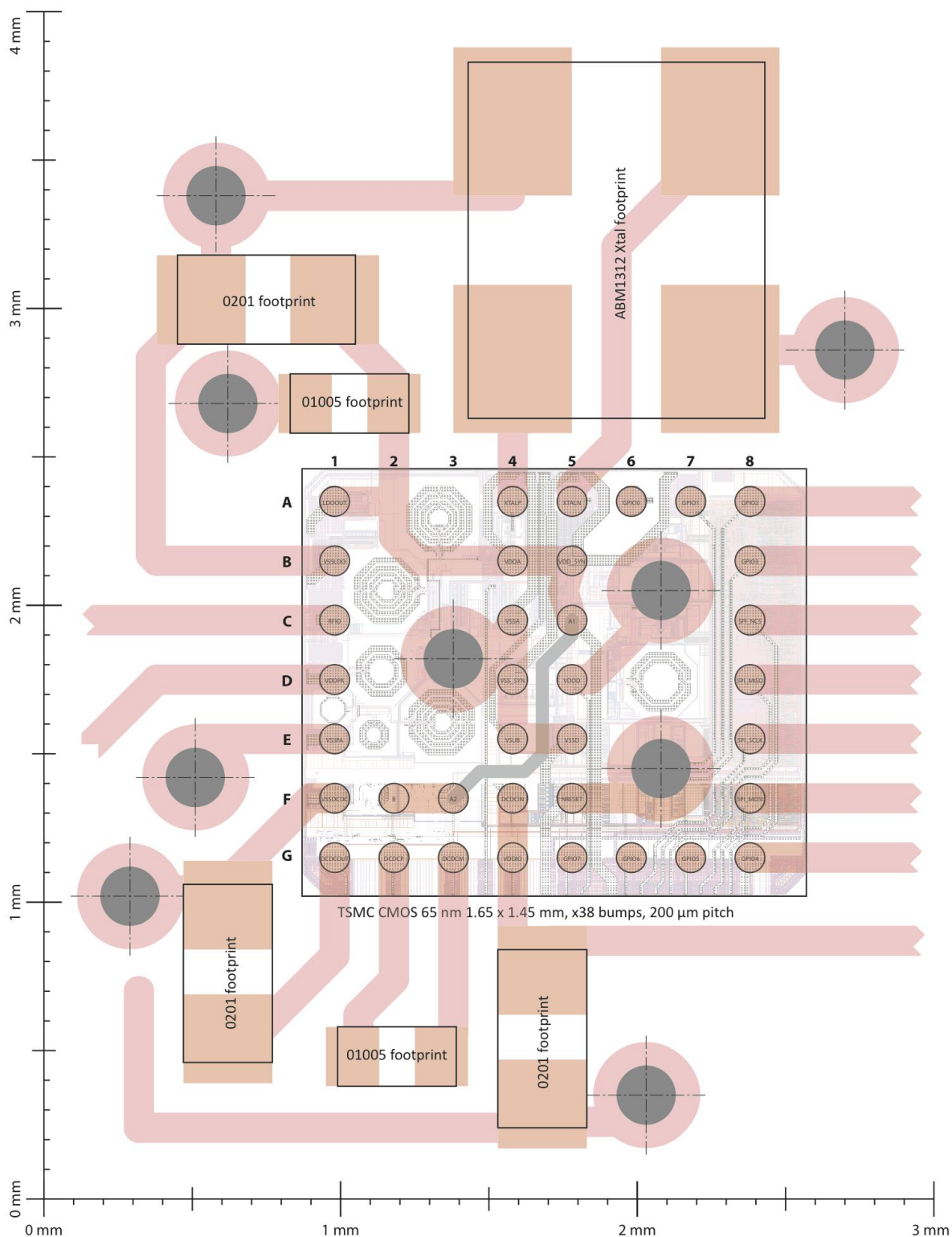


Figure 6: Bottom view of tentative PCB layout of BLIM IC surrounded by associated passives

Ref.	IO Type		Description
A1	A	LDOOUT	Low Dropout voltage regulator output
B1	S	VSSLDO	Low Dropout voltage regulator ground
C1	A	RFIO	50 Ω RF port
D1	S	VDDPA	RF Power Amplifier positive voltage supply
E1	S	VSSPA	RF power amplifier ground
F1	S	VSSDCDC	Capacitive DC-DC voltage converter ground
F2	.	B	Not connected
F3	.	A2	On-chip connected to A1 to help PCB layout
C5	.	A1	On-chip connected to A2 to help PCB layout
G1	A	DCDCOUT	Capacitive DC-DC voltage converter output
G2	A	DCDCP	Capacitive DC-DC voltage converter fly capacitor positive connection
G3	A	DCDCM	Capacitive DC-DC voltage converter fly capacitor negative connection
F4	S	DCDCIN	Capacitive DC-DC voltage converter input positive supply
G4	S	VDDIO	Digital interface positive voltage supply
A4	A	XTALP	Quartz Xtal oscillator positive connection
A5	A	XTALN	Quartz Xtal oscillator negative connection
B4	S	VDDA	Analog positive voltage supply
B5	S	VDD_SYN	RF synthesizer positive voltage supply
C4	S	VSSA	Analog ground
D4	S	VSS_SYN	RF synthesizer ground
D5	S	VSSD	Digital positive voltage supply
E4	S	VSUB	Substrate ground connection
E5	S	VSSD	Digital ground
F5	DI	NRESET	Reset active low
A6	DIO	GPIO0	Digital Input Output
A7	DIO	GPIO1	
A8	DIO	GPIO2	
B8	DIO	GPIO3	
G8	DIO	GPIO4	
G7	DIO	GPIO5	
G6	DIO	GPIO6	
G5	DIO	GPIO5	
C8	DIO	SPI_NCS	SPI Not Chip Select (active low)
D8	DIO	SPI_MISO	SPI Master In Slave Out
E8	DIO	SPI_SCLK	SPI Serial Clock
F8	DIO	SPI_MOSI	SPI Master Out Slave In

Table 4: Preliminary BLIM RF IC IO list

List of Tables

Table 1: IPD module specification summary.....	6
Table 2: Preliminary BLIM module IO list.....	8
Table 3: IPD module specification summary.....	9
Table 4: Preliminary BLIM RF IC IO list.	12

List of Figures

Figure 1: Modules dimensions.	6
Figure 2: BLIM4SME exploded view.	7
Figure 3: Modules PCB footprint.	7
Figure 4: Modules pinning.....	8
Figure 5: Top-level BLIM RF IC circuit block diagram	9
Figure 6: Bottom view of tentative PCB layout of BLIM IC surrounded by associated passives.....	11